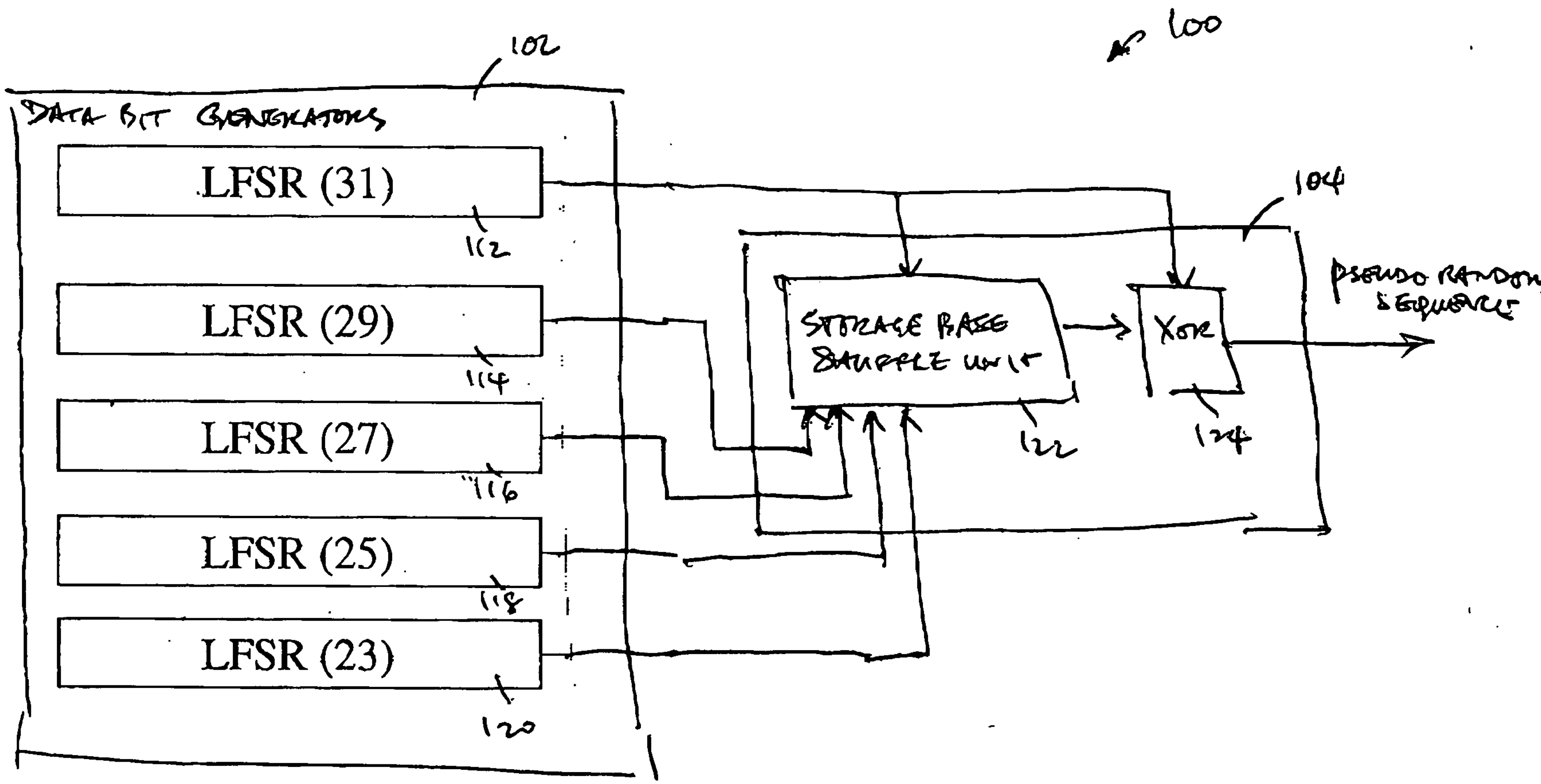
100
102
DATA BIT GENERATORS
LFSR (31)
LFSR (29)
LFSR (27)
LFSR (25)
LFSR (23)
112
114
116
118
120
104
STORAGE BASE SHUFFLE UNIT
122
XOR
124
PSEUDO RANDOM SEQUENCE

FIG. 1

Initialization

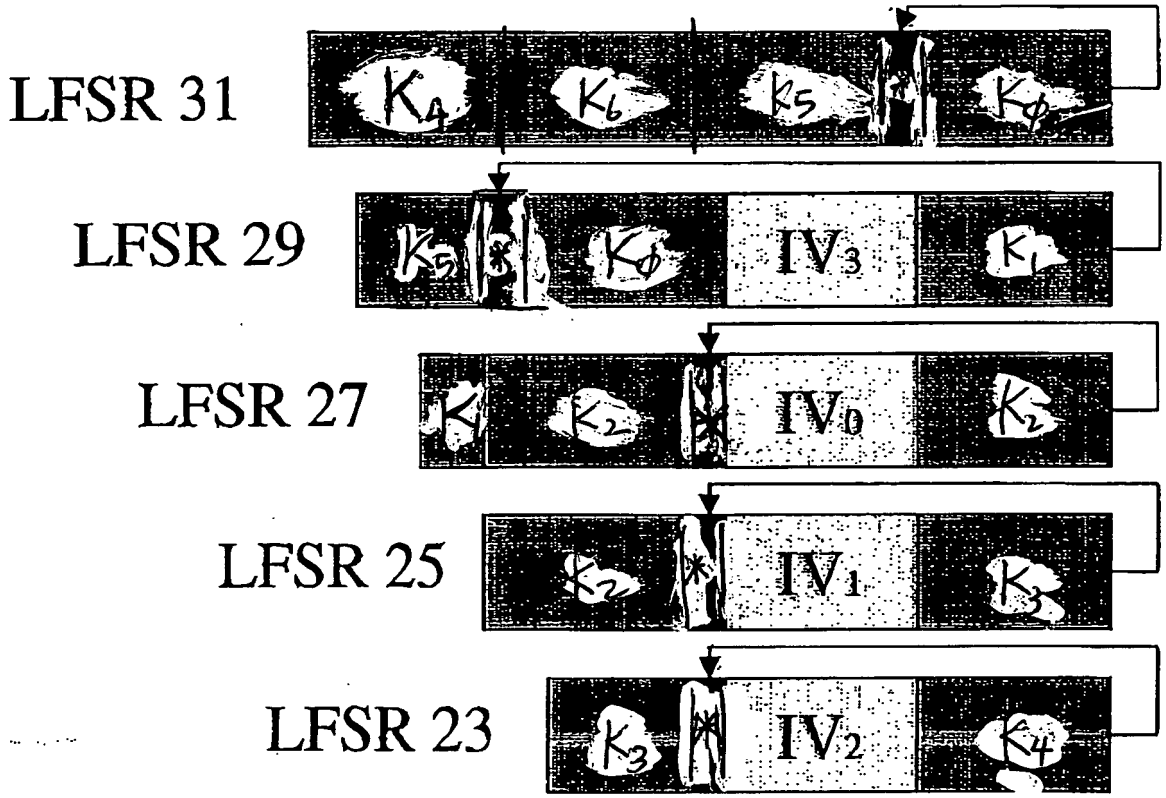

Fig. 2

* Least significant bit of register is complemented

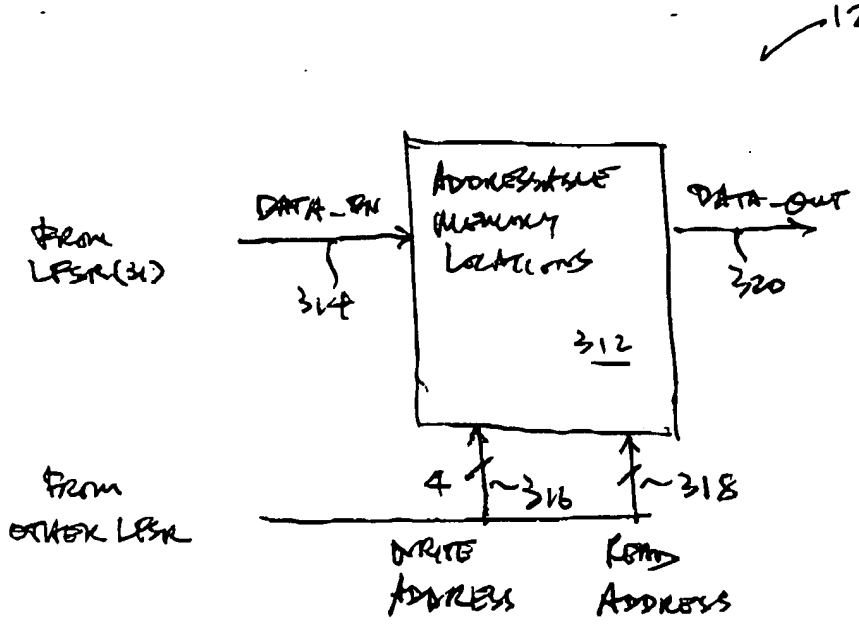
122
DATA_IN
ADDRESSABLE
MEMORY
LOCATIONS
DATA_OUT
FROM
LFSR(31)
314
312
320
FROM
OTHER LFSR
4
316
318
WRITE
ADDRESS
READ
ADDRESS

Fig. 3a

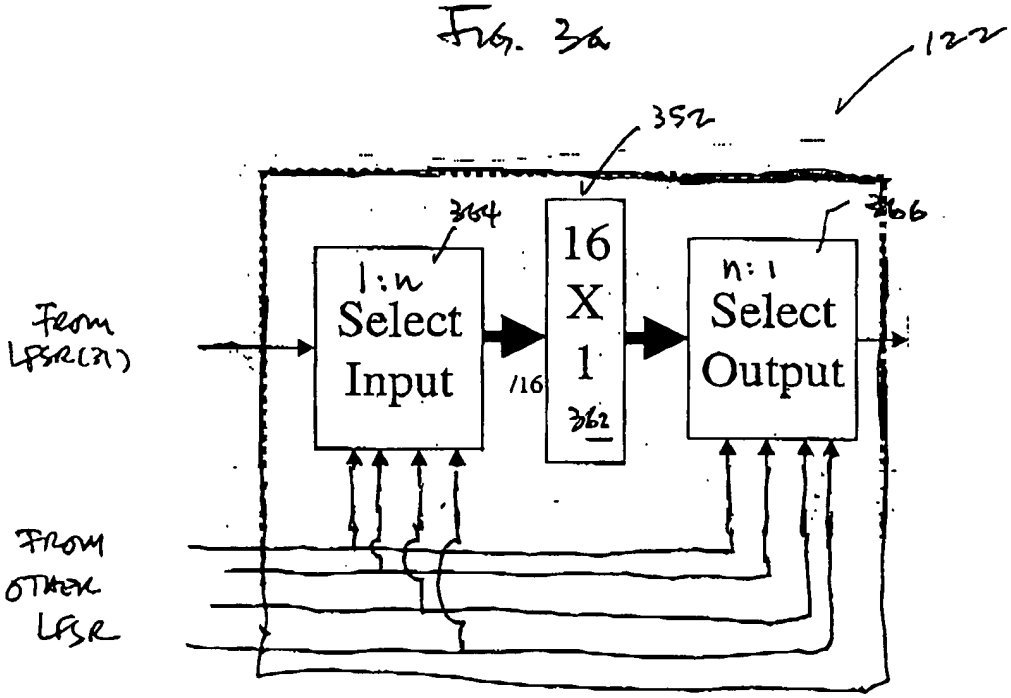
122
352
364
366
1:n
Select
Input
16
X
1
362
116
n:1
Select
Output
FROM
LFSR(31)
FROM
OTHER
LFSR

Fig. 3b